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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,611	09/12/2003	Chun Ho Fan	618902002500	6110

25227 7590 05/16/2007
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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
05/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,611	FAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,15-1-23, 25 and 26* is/are pending in the application.

4a) Of the above claim(s) *18,19 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *13,15-17,20-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 13, 15- 17, 20-22, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/2002/0113308) in view of Melton et al. (US 6,194,250).

Re claim 13, Huang et al. disclose an integrated circuit package comprising: a substrate (20) having a plurality of conductive traces (22) (i.e., i.e., plurality of gold wires **22** which commonly known as **a conductive trace** in the art) (see Fig. 1); a plurality of balls (230) (i.e., the solder balls **230**) disposed on a first surface of the substrate (20) (see Fig. 1); a semiconductor die (21) (i.e., the semiconductor chip **21** and also known as semiconductor die) mounted to the substrate (20) such that bumps (230) of the semiconductor die (21) are electrically connected to

conductive traces of the substrate (see Fig. 1); an overmold material encapsulating (25) (i.e., encapsulant **25**) the semiconductor die (21) and the balls (230) that are disposed farthest form the substrate (20) (see Fig. 1) (see Fig. 1); and a ball grid array (24) disposed on a second surface (i.e., bottom surface) of the substrate (20) and in electrical connection with the conductive traces (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

However, Huang et al. do not disclose specifically show the balls being exposed at an the exterior of the IC package.

Melton et al. disclose an integrated circuit packaging comprising a support (i.e., a substrate) (38) having a plurality of conductive traces (18); a plurality of balls (20) (i.e., metallic bumps) disposed on a first surface of the substrate (38) (see Fig. 4); a semiconductor die (12) mounted to the substrate (38) such that bumps (20) of the semiconductor die (12) are electrically connected to said plurality of conductive traces (18) of the substrate (38); an overmold material (34) encapsulating the semiconductor die (12) and the balls (20) on the substrate (38) such that portions of said balls (20) that are disposed farthest from the substrate (38) are exposed at an exterior of the integrated circuit package (see Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

As Melton et al. disclose that "the resulting polymeric body 14 encapsulates active face **28** of integrated circuit die **12**, the plurality of wire leads **18**, inner surface **19**, and metallic bumps **20**, thereby protecting them from environmental exposure and damage experienced during normal use of microelectronic package **10.** Second surface **26** is formed opposite first surface **24** by the surface tension of the polymeric precursor. In a preferred embodiment, first

surface 24, non-active face **32**, and outer surface 17 cooperate to form planar surface 37. Planar surface 37 facilitates the manipulation of microelectronic assembly **10** by conventional robotic end effectors having vacuum pickup ends or the like. Bonding surface **30** of each metallic bump **20** is exposed at second surface **26** of polymeric body **14** and protrudes from second surface **26** to provide a surface capable of forming reliable solder interconnections. The exposure of bonding surface **30** provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like." (See Melton et al. Col. 4, lines 36-55).

Both Huang et al. ' 0113308 and Melton et al. '250 teachings are directed to semiconductor device package and the package includes the ball grid array and over mold resin. Therefore, the teachings of Huang et al. ' 0113308 and Melton et al. '250 are analogous. Hence, one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful structure a plurality of balls being exposed at an the exterior of the IC package as disclosed by Melton et al. '250 in order to provide a surface capable of forming reliable solder interconnections and the exposure of bonding surface provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. reference with a plurality show the balls being exposed at an the exterior of the IC package as taught by Melton et al. in order to provide a surface capable of forming reliable solder interconnections and the exposure of bonding surface provides a bonding surface that is able to be attached to solder bumps or bond pads on a printed circuit board or the like.

Re claim 15, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of balls (230) is attached to respective solder ball pads (see Abstract) on the first surface of the substrate (i.e., top surface) (20) (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 16, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the bumps (i.e., the ball grid array **24**) of the semiconductor die (21) are electrically connected to the conductive traces (22) by wire bonds (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 17, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the semiconductor die is fixed to the first surface of the substrate (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 20, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of balls circumscribe the semiconductor die (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 21, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of balls

electrically connected to the conductive traces of the substrate (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 22, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the balls are deformed (i.e., the solder balls 230 are formed by reflow that requires deformation process) (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 24, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation further comprising a heat spreader (231) mounted to the balls (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

Re claim 25, as applied to claim 13 above, Huang et al. and Melton et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of balls is comprised of a plurality of solder balls (See Huang et al. Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]; and Melton et al. Figs. 4-7 and related text Col. 3, line 23 – Col. 5, line 28).

3. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/2002/0113308) and Melton et al. (US 6,194,250), as applied in Paragraph 2 above, and in further view of Huang et al. (US/6,707,167).

Re claim 23, Huang et al. and Melton et al. disclose all the claimed limitations except a die adapter mounted on said semiconductor die and encapsulated in the overmold material.

Huang et al. '167 disclose an IC package that a die adopter (16) that is mounted on the semiconductor die (12) which encapsulated in the overmold material (14) (see Fig. 2). As Huang et al. '167 disclose the die adopter 16 prevents cracking of the IC die (see Col. 3, lines 38-55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. '0113308 and Melton et al. reference with die adopter as taught by Huang et al. '167 in order to prevent die cracking.

Response to Arguments

4. Applicants' arguments with respect to claims 13, 15-17, 20-23, and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
May 14, 2007